DETAILED ACTION

1. Claims 1-4 and 11-22 are pending in this office action.

2. Applicant's arguments, filed June 19, 2008, have been fully considered but they are not persuasive.

Claim Rejections

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. Claims 1-4 and 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa (U.S. Patent No. 5,117,380) in view of Feyt et al. (U.S. Patent No. 6,698,662).

Regarding claims 1, 3, 11 and 13: Tanagawa discloses a data processing apparatus/memory card comprising:

- An operation processing unit (col. 2, lines 11-19, the integrated circuit) connected to a data bus (fig. 1, ref. num 9) and configured to perform a read cycle by outputting a read control signal to a memory (col. 2, lines 51-54) to read a read data word output by said memory to said data bus, and a write cycle by

outputting a write control signal to said memory and a write data word to said data bus to write said data word in the memory (fig. 2 and col. 2, lines 40-50); and

- A pseudo-data generating circuit connected to said data bus (fig. 1, ref. num 5 and 6), said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit (col. 2, lines 40-50), said pseudo-data generating circuit configured to generate pseudo-data and output the generated pseudo-data to said data bus according to an output timing based on said read control signal and said write control signal output from said operation processing unit (fig. 2 and col. 3, lines 8-18).

Tanagawa doesn't explicitly disclose the output timing controlled to occur between a read cycle and an immediately following write cycle, between a write cycle and an immediately following read cycle, between a read cycle and an immediately following read cycle, or between a write cycle and an immediately following write cycle.

However Feyt et al. discloses a method for hiding operation performed by microprocessor card where he teaches presenting a random data items on the data bus during cryptographic calculation like read and write operations (col. 2, lines 36-42 and col. 3, lines 34-52).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the Tanagawa system with the teaching of Feyt to output pseudo-data on the data bus between read and write cycles. One would be motivated to do so in order to mask the power consumption by the memory during the reading or writing of secret data to prevent an attacker from deducing the data by correlation or differential power analysis attacks (see col. 1, lines 36-46 of Feyt et al.).

Regarding claims 2, 4, 12 and 14: Tanagawa as modified by Feyt et al. discloses wherein said pseudo-data generating circuit generates random number data as the pseudo-data (see col. 2, lines 9-19 of Tanagawa).

Regarding claims 15, 17, 19, and 21: Tanagawa as modified by Feyt et al. discloses wherein the operation processing unit is further configured to output the read control signal to have an active read control time period and an inactive read control time period, and output the write control signal to have an active write control time period and an inactive write control time period (see col. 3, lines 19-21 of Tanagawa), and the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to prevent the output of the generated pseudo-data to the data bus during at least one of the active read control time period and the active write control time period (see col. 3, lines 21-26 of Tanagawa).

Regarding claims 16, 18, 20, and 22: Tanagawa as modified by Feyt et al. discloses wherein the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period (see fig. 2, ref. num T2 of Tanagawa).

Response to Arguments

5. Applicant argues that the combination of references fail to teach a pseudo-generating circuit connected to said bus and configured to generate pseudo-data and output the pseudo-data to said bus according to output timing between read and write cycles (page 3 and top of page 4). Applicant has similar arguments for claim 3.

Regarding applicant's argument, examiner disagrees. First, the elements which make up the pseudo-data generating circuit are shown in figure 1 as elements 1-8. The oscillators (1 and 3) are taught to be separate from the system clock, which is part of the circuit (col. 2, lines 20-28); however, the remaining elements (2 and 4-8) are all part of the circuit and control the generation of pseudo-data. Second, the claim calls for output timing controlled to occur between read and write, write and read, read and read, OR write and write. Figure 2 of Tanagawa clearly shows output timing based on two read cycles. The arguments for claim 3 are addressed above since they are similar to claim 1.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. HOFFMAN whose telephone number is (571)272-3863. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser G. Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Brandon S Hoffman/
Primary Examiner, Art Unit 2136